



**Christu Jyothi Institute of Technology & Science**  
Colombonagar, Yeshwanthapur, Jangaon

**Department of Electronics and Communication Engineering**  
2022-23 2<sup>nd</sup> Semester  
**LESSION PLAN**

**Department: ECE**

**Faculty Name: Mr. HANUMANTHU.B**

**Year &Section: III/II**

**Academic Year: 2022-2023**

**Subject: VLSI DESIGN**

**Subject Code : EC603PC**

<b>Lect No.</b>	<b>Topic</b>	<b>Teaching Aids</b>	<b>Reference</b>
	<b><u>UNIT:1</u></b> Introduction to VLSI		
1.	Introduction to IC Technology	TM1/TM2/TM7/TM11	T1/R1
2.	MOS Transistor, Enhancement and Depletion Mode	TM1/TM2/TM11	T1/R1
3.	MOS Fabrication Process	TM1/TM2/TM7	T1/R1
4.	Fabrication Process :NMOS,PMOS	TM1/TM2/TM7	T1/R1
5.	Fabrication Process :CMOS	TM1/TM2/TM7	T1/R1
6.	Berkeley n-well Process ,Twin Tub Process	TM1/TM2	T1/R1
7.	Fabrication Process :BICMOS	TM1/TM2	T1/R1
8.	BICMOS	TM1/TM2	T1/R1
9.	Latch up susceptibility	TM1/TM2	T1/R1
10.	Oxidation, Lithography, Diffusion	TM1/TM2	T1/R1
11.	Ion implantation, Metallization, Encapsulation	TM1/TM2	T1/R1
12.	Probe testing, Integrated Resistors and Capacitors	TM1/TM2	T1/R1
13.	CMOS Nanotechnology	TM1/TM2	T1/R1
14.	Tutorial class on unit 1 -revision	TM1/TM2	T1/R1

15.	BASIC ELECTRICAL PROPERTIES : Basic Electrical Properties of MOS and BiCMOS Circuits: Ids-Vds relationships	TM1/TM2	T1/R1
16.	MOS transistor threshold Voltage	TM1/TM2	T1/R1
17.	gm, gds, figure of merit $\eta$ ; Pass transistor, NMOS Inverter	TM3	T1
	NMOS Inverter		
18.	Various pull ups	TM1/TM2/TM7	T1/R1
19.	CMOS Inverter analysis and design	TM1/TM2/TM7	T1/R1
20.	Bi-CMOS Inverters	TM1/TM2/TM7	T1/R1
21.	Tutorial class on unit 2 -revision	TM1/TM2/TM7/T M11	T1/R1
22.	<b>UNIT-II: VLSI CIRCUIT DESIGN PROCESSES :</b> VLSI CIRCUIT DESIGN PROCESSES :	TM1/TM2/TM7	T1/R1
23.	VLSI Design Flow	TM1/TM2/TM7	T1/R1
24.	MOS Layers, Stick Diagrams	TM1/TM2/TM11	T1/R1
25.	Stick Diagrams	TM1/TM2/TM7	T1/R1
26.	Design Rules and Layout	TM1/TM2/TM7	T1/R1
27.	2 nm CMOS Design rules for wires	TM1/TM2/TM7	T1/R1
28.	Contacts and Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates	TM1/TM2/TM11	T1/R1
29.	Scaling of MOS circuits	TM3	T1
	Tutorial class on unit3 -revision		
30.	<b>UNIT-III :GATE LEVEL DESIGN :</b> Logic Gates and Other complex gates	TM1/TM7	T1/R1
31.	Switch logic, Alternate gate circuits	TM1/TM2/TM11	T1/R1
32.	Gallium Arsenide Devices	TM1/TM2/TM7/T M11	T1/R1
33.	Time Delays	TM1/TM2/TM7/T M11	T1/R1
34.	Driving large Capacitive Loads, Wiring Capacitances, Fan-in and fan-out, Choice of layers	TM1/TM2/TM7/T M11	T1/R1
35.	Tutorial class on unit4 -revision	TM1/TM2/TM7/T	T1/R1

		M11	
36.	<b>UNIT-IV:</b> SUBSYSTEM DESIGN : Subsystem Design, Shifters	TM1/TM2/TM7/T M11	T1/R1
37.	Adders, ALUs	TM1/TM2/TM7/T M11	T1/R1
38.	Multipliers, Parity generators	TM1/TM2/TM7/T M11	T1/R1
39.	Comparators, Zero/One Detectors, Counters	TM3	T1
	Tutorial class on unit5 -revision		
40.	Array Subsystems :SRAM,DRAM	TM1/TM2/TM7	T1/R1
41.	ROM, Serial Access Memories	TM1/TM2/TM7	T1/R1
42.	Dynamic Register Element	TM1/TM2/TM7	T1/R1
43.	Content Addressable Memory	TM1/TM2/TM7	T1/R1
44.	Tutorial class on unit6 -revision	TM1/TM2/TM7	T1/R1
45.	<b>UNIT-V:</b> SEMICONDUCTOR INTEGRATED CIRCUIT DESIGN : PLAs	TM1/TM2/TM7	T1/R1
46.	FPGAs	TM1/TM2/TM7	T1/R1
47.	CPLDs	TM1/TM2/TM7	T1/R1
48.	Standard Cells, Programmable Array Logic	TM1/TM2/TM7	T1/R1
49.	System Partitioning Missing	TM1/TM2/TM7	T1/R1
50.	Design Approach	TM3	T1
	Parameters influencing low power design	TM1/TM2/TM7	T1/R1
51.	Tutorial class on unit 7 -revision	TM1/TM2/TM7	T1/R1
52.	CMOS TESTING : CMOS Testing	TM1/TM2/TM7	T1/R1
53.	Need for testing	TM1/TM2/TM7	T1/R1
54.	Test Principles	TM1/TM2/TM7	T1/R1
55.	Design Strategies for test	TM1/TM2/TM7	T1/R1
56.	Chip level Test Techniques	TM1/TM2/TM7	T1/R1

57.	System-level Test Techniques	TM1/TM2/TM7	T1/R1
58.	Layout Design for improved Testability. and Tutorial class on unit8 -revision	TM1/TM2/TM7	T1/R1
59.	Revision of previous papers	TM1/TM2/TM7	
60.	Revision of previous papers	TM1/TM2/TM7	
61.	Revision of previous papers	TM1/TM2/TM7	
62.	Revision of previous papers	TM1/TM2/TM7	
TM1: Chalk and talk		TM2: PPT	TM3:Seminar
TM5: Lab Demos		TM6: Audio Visual Aids	TM7:Group Discussion
TM9: 3D models		TM10: Puzzle	TM11: Quiz
TM13: Case Study		TM14: Flash Cards	TM15:Text Book Assignment
TM17: Surveys		TM18: Open Text Book Test	TM19: Cross Word Puzzles
TM21: Individual Projects			
			TM4: Webinar
			TM8: Field Visits
			TM12: Industrial Visits
			TM16: Role Play
			TM20: Debates

**TEXT BOOKS:**

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Douglas and A. Pucknell, PHI, 2005 Edition
2. CMOS VLSI Design – A Circuits and Systems Perspective, Neil H. E Weste, David Harris, Ayan Banerjee, 3rd Ed, Pearson, 2009.

**REFERENCE:**

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. CMOS logic circuit Design - John. P. Uyemura, Springer, 2007
3. Modern VLSI Design - Wayne Wolf, Pearson Education, 3rd Edition, 1997.

**Date**

**Signature of the faculty**